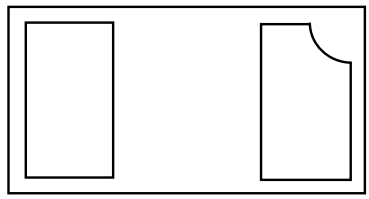
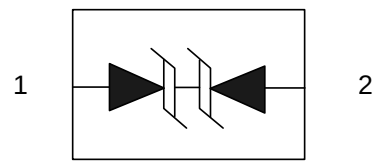
Feature

- 200W peak pulse power per line (t_P = 8/20μs)
- DFN1006-2L package
- Replacement for MLV(0402)
- Bidirectional configurations
- Response time is typically < 1ns
- Low clamping voltage
- RoHS compliant
- Transient protection for data lines to
  IEC61000-4-2(ESD） ±20KV(air), ±20KV(contact);
  IEC61000-4-4 (EFT) 40A (5/50ns)

DFN1006-2L



PIN CONFIGURATION



Applications

- Cellular phones
- Portable devices
- Digital cameras
- Power supplies

Mechanical Characteristics

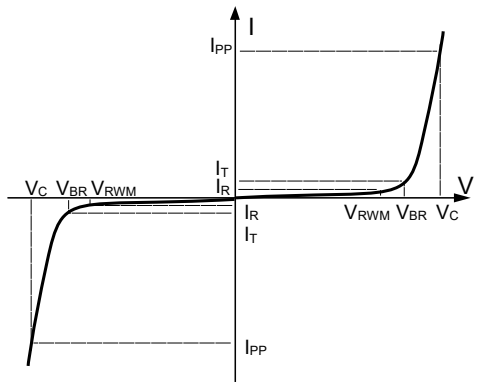
- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260℃
- Device meets MSL 1 requirements
- Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{pp}	200	W
Operating Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				24	V
Breakdown Voltage	V_{BR}	I_t = 1mA	25	27		V
Reverse Leakage Current	I_R	V_{RWM} = 24V T=25℃			1.0	μA
Clamping Voltage	V_C	I_{PP}=1A		34	40	V
Clamping Voltage	V_C	I_{PP}= 4A		52	58	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		10	13	pF

Typical Characteristics

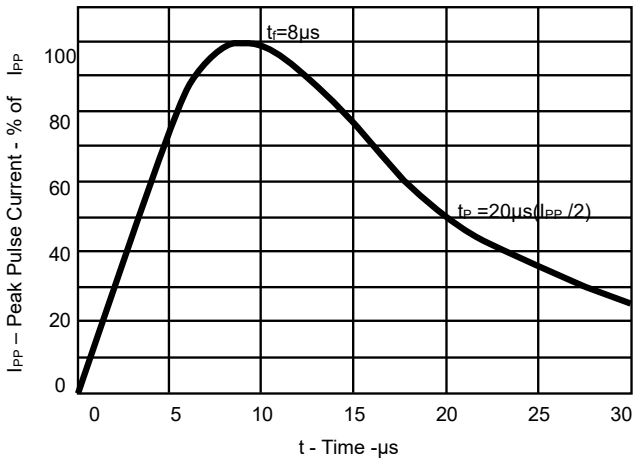


Fig 1.Pulse Waveform

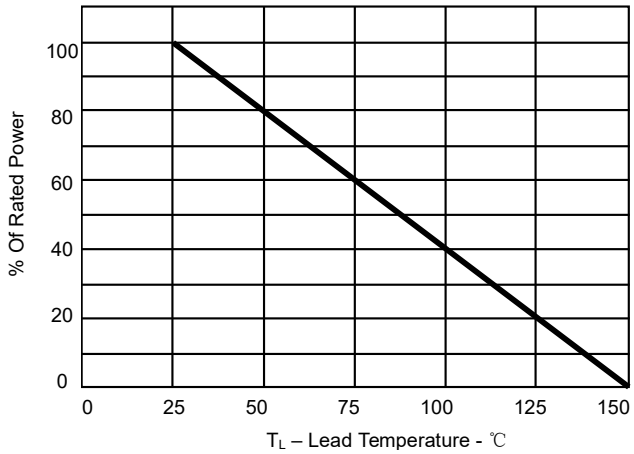


Fig 2.Power Derating Curve

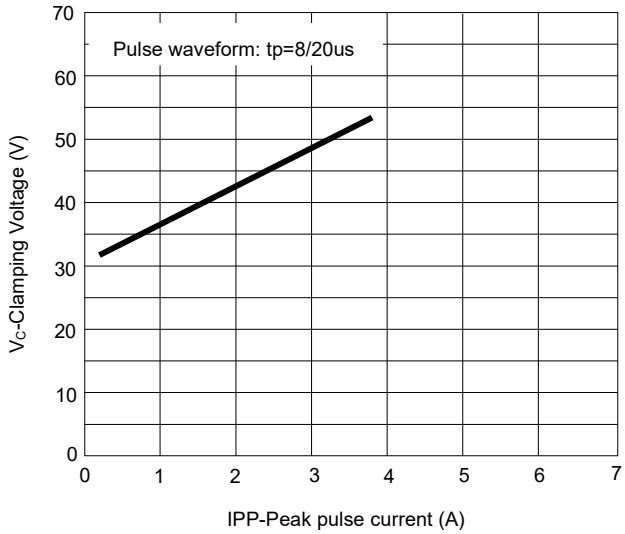


Fig 3. Clamping voltage vs. Peak pulse current

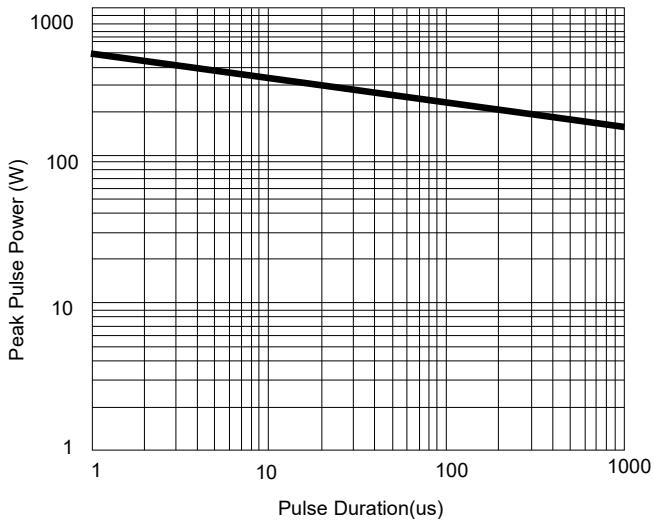
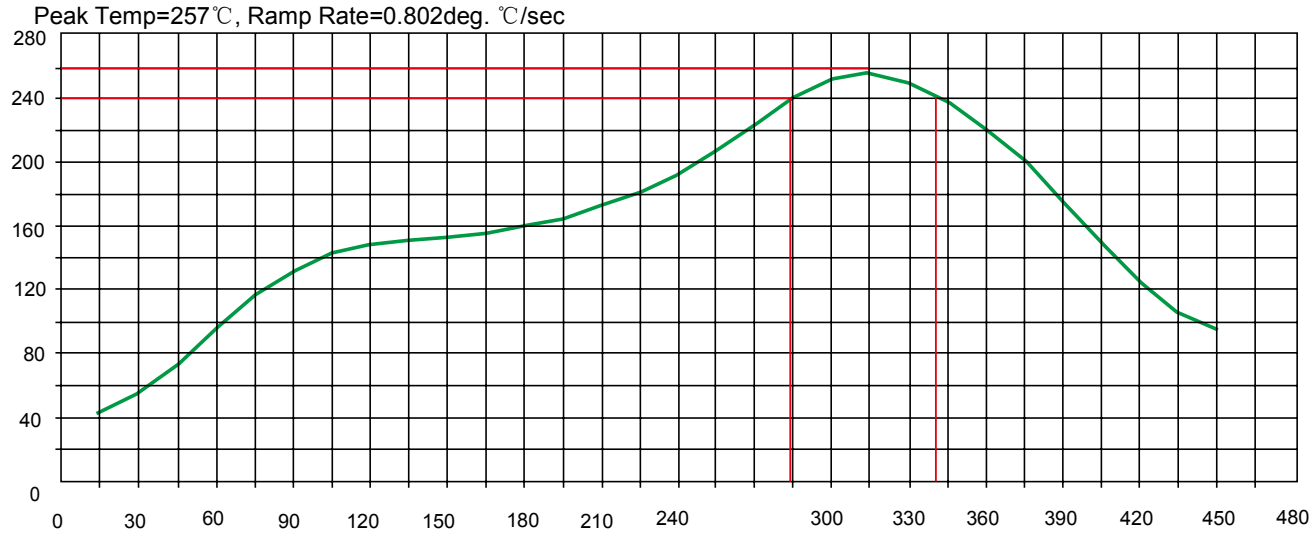


Fig 4. Non-Repetitive Peak Pulse Power vs. Pulse time

Solder Reflow Recommendation

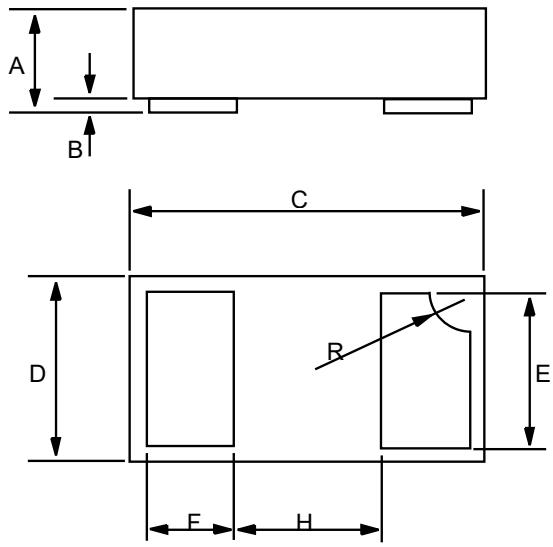


PCB Design

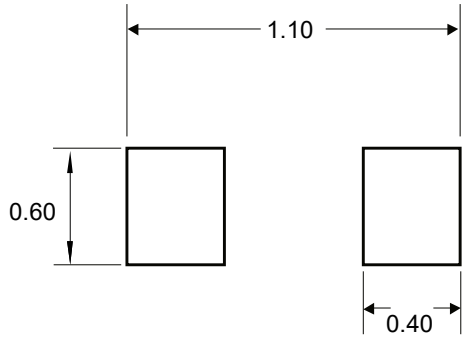
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (DFN1006-2L)



Dim	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.013	0.020	0.34	0.50
B	0.000	0.002	0.00	0.05
C	0.037	0.043	0.95	1.080
D	0.022	0.027	0.55	0.680
E	0.016	0.024	0.40	0.60
F	0.008	0.012	0.20	0.30
H	0.015Typ.		0.40Typ.	
R	0.001	0.005	0.05	0.15



Unit:mm

Suggested PCB Layout