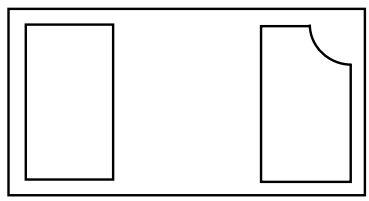
Feature

♦100W peak pulse power per line (tP = 8/20μs)
♦DFN1006-2L package
♦Replacement for MLV(0402)
♦Bidirectional configurations
♦Response time is typically < 1ns
♦Low clamping voltage
♦RoHS compliant
♦Transient protection for data lines to
IEC61000-4-2(ESD) ±15KV(air), ±12KV(contact);
IEC61000-4-4 (EFT) 40A (5/50ns)

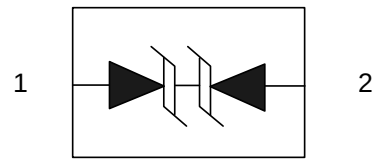
DFN1006-2L



Applications

♦Cellular phones
♦Portable devices
♦Digital cameras
♦Power supplies

PIN CONFIGURATION



Mechanical Characteristics

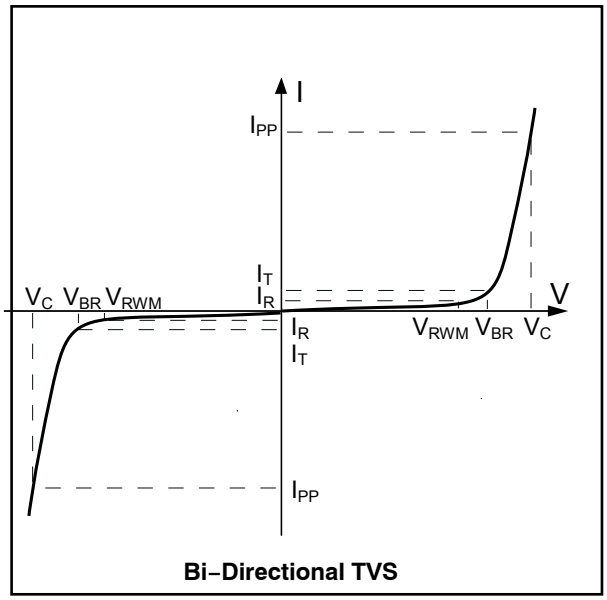
♦Lead finish:100% matte Sn(Tin)
♦Mounting position: Any
♦Qualified max reflow temperature:260℃
♦Device meets MSL 2 requirements
♦Pure tin plating: 7 ~ 17 um
♦Pin flatness:≤3mil

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (tp=8/20μs)	Ppp	100	W
Operating Temperature	TJ	-55 to +150	℃
Storage Temperature	TSTG	-55 to +150	℃

ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Bi-Directional TVS

Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Units
Peak Reverse Working Voltage	VRWM				5	V
Breakdown Voltage	VBR	It = 1mA	5.6		8.5	V
Reverse Leakage Current	IR	VRWM = 5V T=25℃			1	μA
Maximum Reverse Peak Pulse Current	IPP			5.5		A
Clamping Voltage	VC	IPP=1A			10	V
Clamping Voltage	VC	IPP=3A			15	V
Clamping Voltage	VC	IPP=5A			21	V
Junction Capacitance	Cj	VR=0V f = 1MHz		0.3	0.5	pF

Typical Characteristics

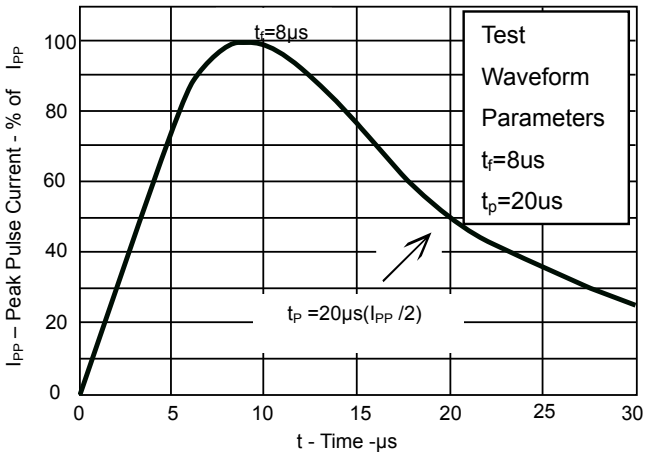


Fig 1.Pulse Waveform

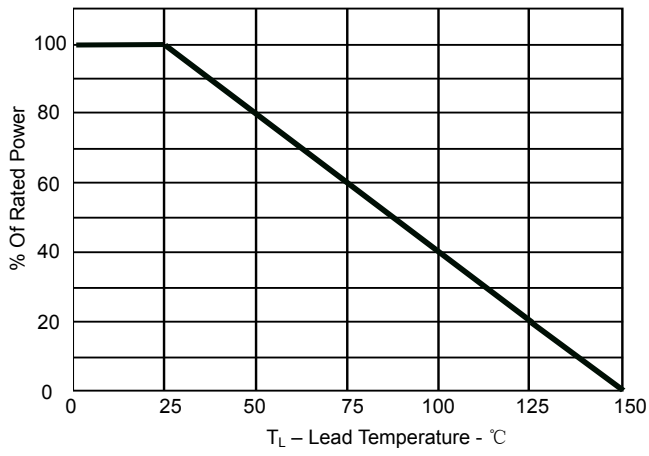


Fig 2.Power Derating Curve

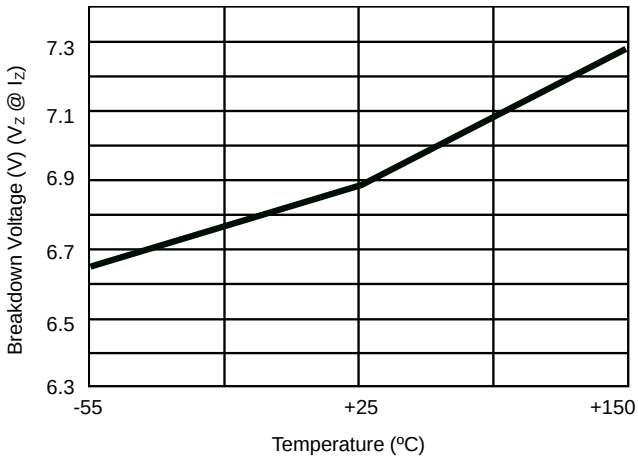


Fig 3.Typical Breakdown Voltage vs. Temperature

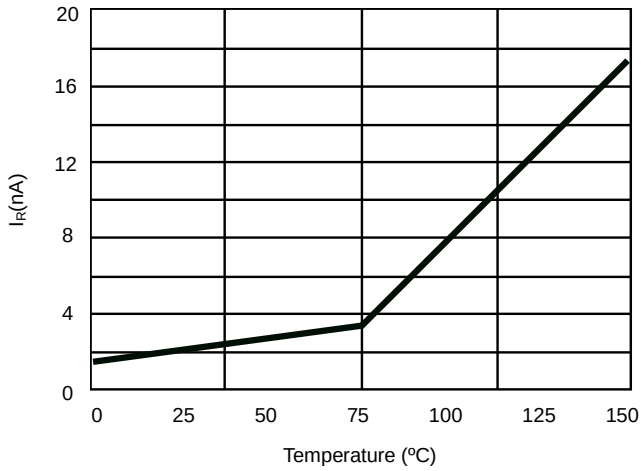


Fig 4.Typical Leakage Current vs. Temperature

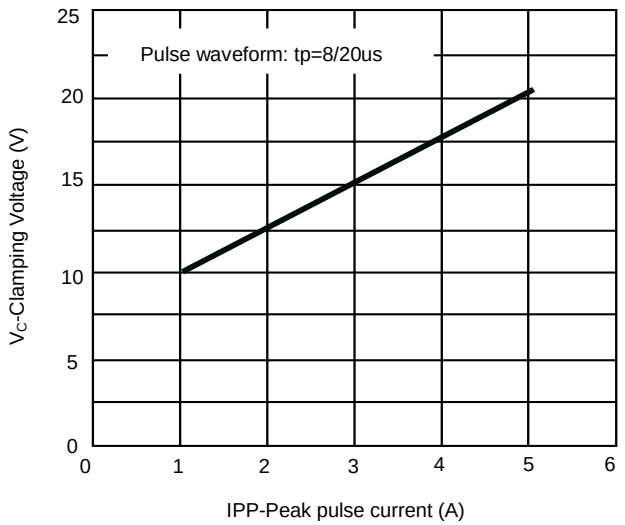


Fig 5. Clamping voltage vs. Peak pulse current

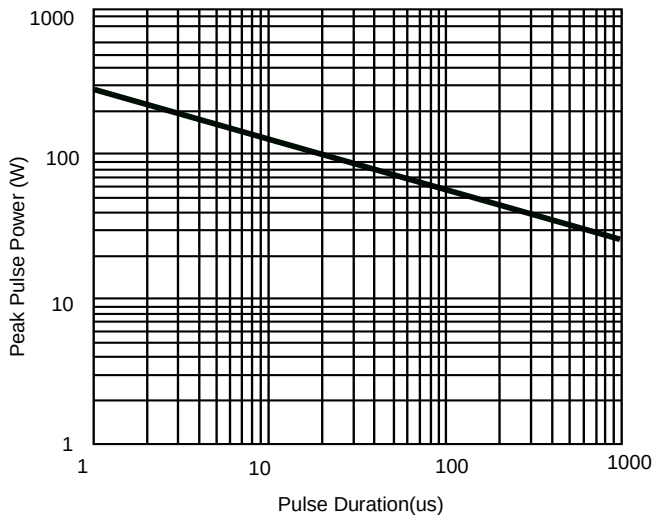


Fig 6. Non-Repetitive Peak Pulse Power vs. Pulse time

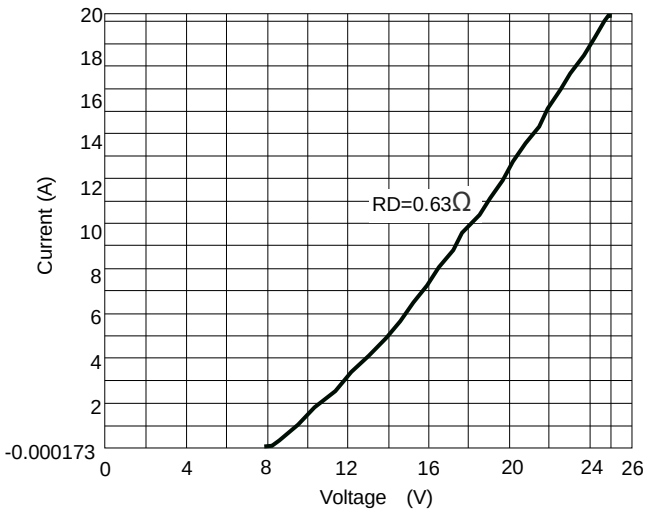
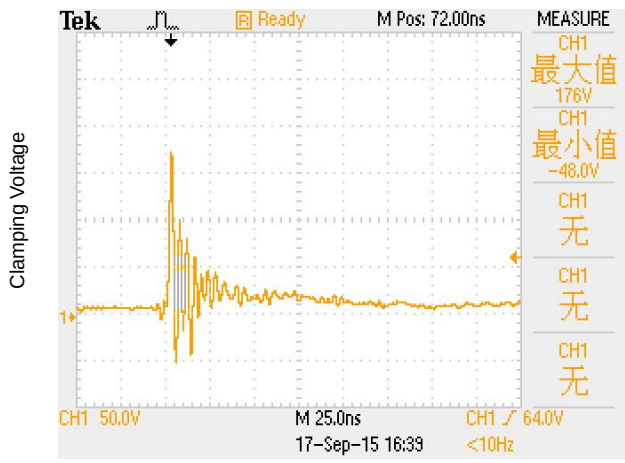


Fig 7. TLP Measurement

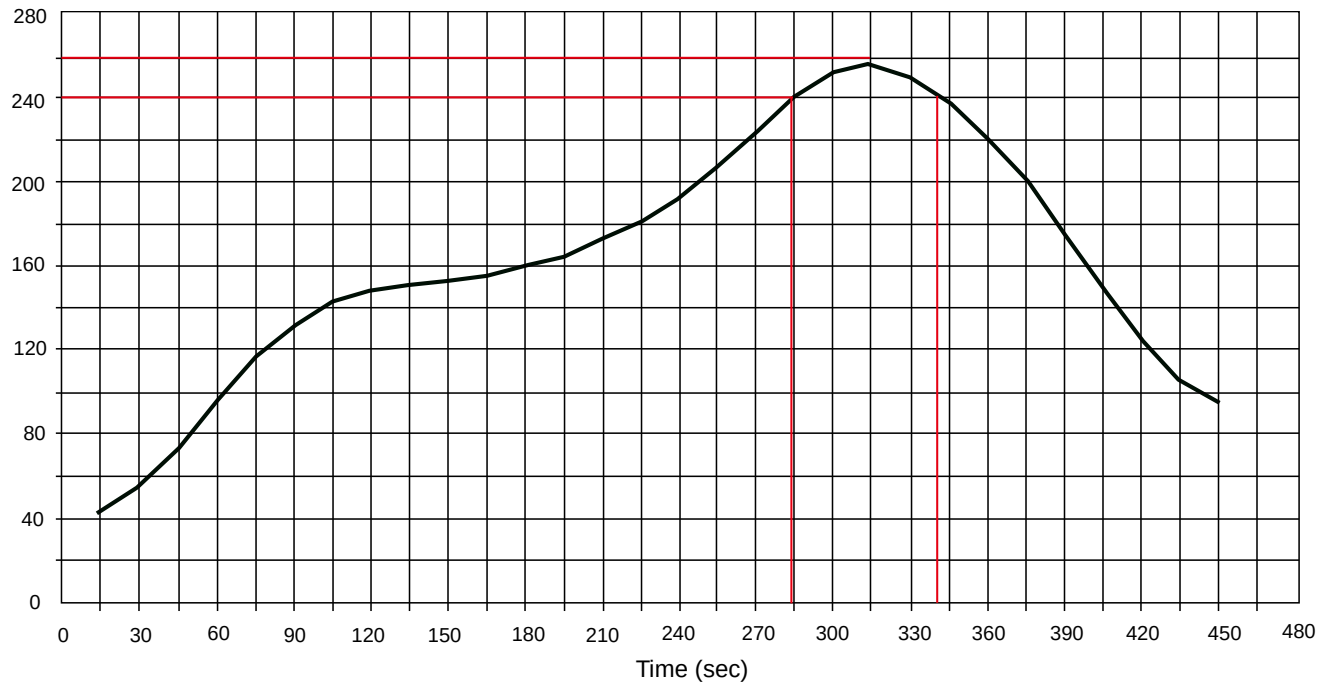


ESD clamping

Fig 8 (8kV contact discharge per IEC61000-4-2)

Solder Reflow Recommendation

Peak Temp=257℃, Ramp Rate=0.802deg. ℃/sec

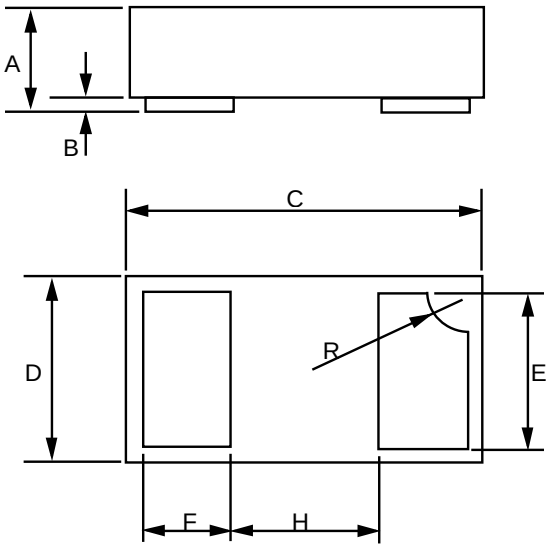


PCB Design

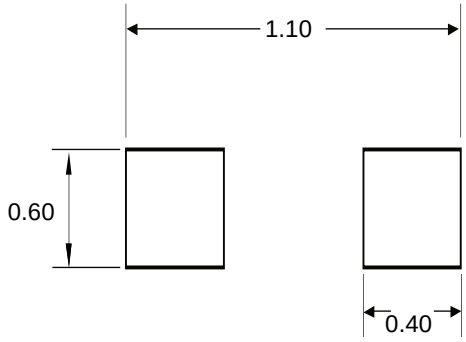
For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (DFN1006-2L)



Dim	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.013	0.020	0.34	0.50
B	0.000	0.002	0.00	0.05
C	0.037	0.042	0.95	1.075
D	0.021	0.026	0.55	0.675
E	0.017	0.021	0.45	0.55
F	0.007	0.011	0.20	0.30
H	0.015Typ.		0.40Typ.	
R	0.001	0.005	0.05	0.15



Unit:mm