



## 1-Line, Bi-directional, Ultra-low Capacitance Transient Voltage Suppressors

### Features

- Stand-off voltage: 5V Max.
- Transient protection for each line according to IEC61000-4-2 (ESD):  $\pm 30\text{kV}$  (contact discharge) IEC61000-4-5 (surge): 11A (8/20 $\mu\text{s}$ )
- Ultra-low capacitance:  $C_J = 0.8\text{pF}$  typ.
- Ultra-low leakage current:  $I_R < 1\text{nA}$  typ.
- Low clamping voltage:  $V_{CL} = 7.5\text{V}$  typ. @  $I_{PP} = 16\text{A}$  (TLP)
- Solid-state silicon technology

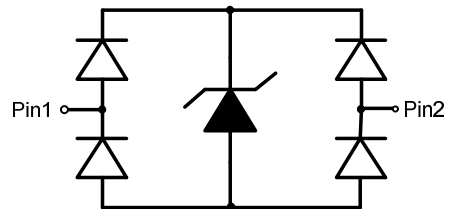
### Applications

- USB 2.0 and USB 3.0
- HDMI 1.3 and HDMI 1.4
- SATA and eSATA
- DVI
- IEEE 1394
- PCI Express
- Portable Electronics
- Notebooks

### DFN1006-2L



### Circuit Diagram



Marking	Packaging
E	10,000/Tape & Reel

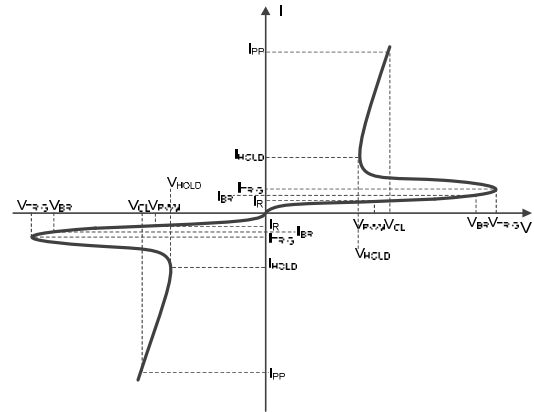
### Absolute maximum rating@25°C

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_P = 8/20\mu\text{s}$ )	$P_{PP}$	100	W
Peak Pulse Current ( $t_P = 8/20\mu\text{s}$ )	$I_{PP}$	11	A
Lead Soldering Temperature	$T_L$	260 (10 sec)	°C
Operating Temperature	$T_J$	-40 to 85	°C
Storage Temperature	$T_{STG}$	-55 to 150	°C
ESD according to IEC61000-4-2 air discharge	$V_{ESD}$	$\pm 30$	KV
ESD according to IEC61000-4-2 contact discharge		$\pm 30$	



### Electrical characteristics (TA=25 °C, unless otherwise noted)

- V<sub>RWM</sub> Reverse stand-off Voltage
- I<sub>R</sub> Reverse leakage current
- V<sub>CL</sub> Clamping voltage
- I<sub>PP</sub> Peak pulse current
- V<sub>TRIG</sub> Reverse trigger voltage
- I<sub>TRIG</sub> Reverse trigger current
- V<sub>BR</sub> Reverse breakdown voltage
- I<sub>BR</sub> Reverse breakdown current
- V<sub>HOLD</sub> Reverse holding voltage
- I<sub>HOLD</sub> Reverse holding current



### Electrical characteristics (T<sub>A</sub>=25 °C, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V <sub>RWM</sub>				5.0	V
Reverse leakage current	I <sub>R</sub>	V <sub>RWM</sub> = 5V		<1	50	nA
Reverse breakdown voltage	V <sub>BR</sub>	I <sub>T</sub> = 1mA	7.0			V
Clamping voltage	V <sub>CL</sub>	I <sub>PP</sub> = 16A, t <sub>p</sub> = 100ns		7.5		V
Dynamic resistance	R <sub>DYN</sub>			0.20		Ω
Clamping voltage	V <sub>CL</sub>	V <sub>ESD</sub> = 8kV		7.5		V
Clamping voltage	V <sub>CL</sub>	I <sub>PP</sub> = 1A, t <sub>p</sub> = 8/20μs			5.0	V
		I <sub>PP</sub> = 11A, t <sub>p</sub> = 8/20μs			9.0	V
Junction capacitance	C <sub>J</sub>	V <sub>R</sub> = 0V, f = 1MHz		0.8	1.0	pF

Fig 1.8/20μs waveform per IEC61000-4-5

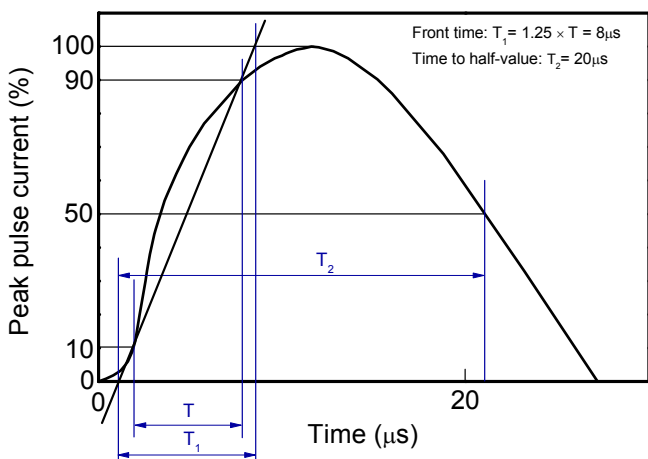
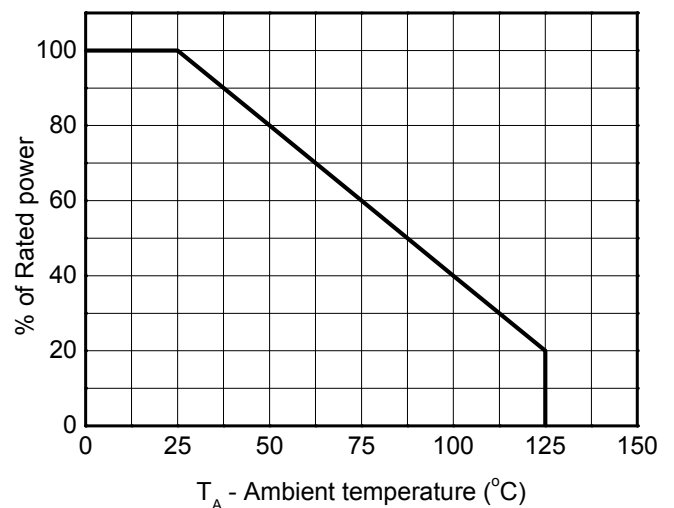
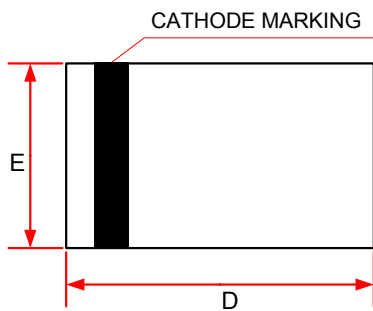


Fig 2. Power derating vs. Ambient temperature

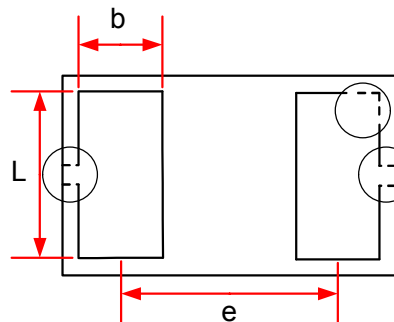




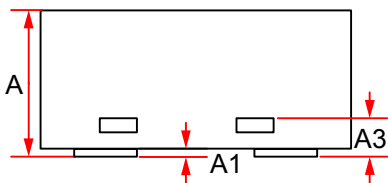
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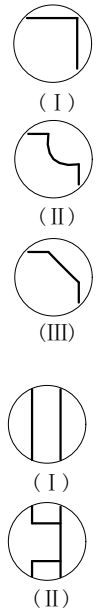
Top View



Bottom View

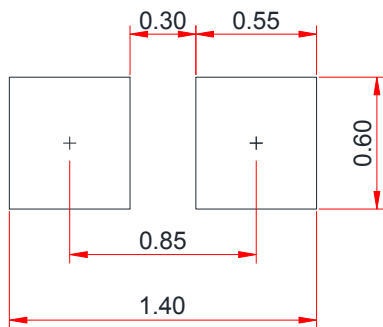


Side View



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.340	0.450	0.530
A1	0.000	0.020	0.050
A3	0.125 Ref.		
D	0.950	1.000	1.075
E	0.550	0.600	0.675
b	0.200	0.250	0.300
L	0.450	0.500	0.550
e	0.650 BSC		

### Recommended PCB Layout (Unit: mm)



#### Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.



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