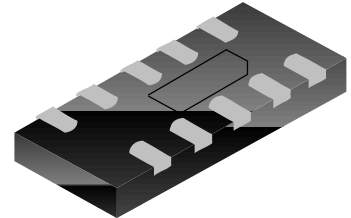




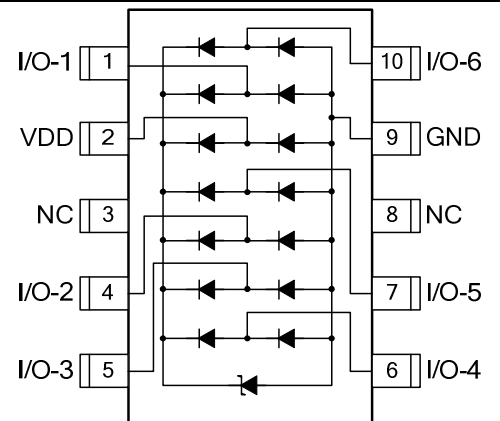
ESD14N5V0U6U TVS arrays designed to protect power/control lines and high-speed signal lines from overvoltage hazard of Electrostatic Discharge (ESD), Electrical Fast Transients (EFT) and Lightning. These interfaces can be used for high definition multi-media interface (HDMI) at 1.65 Gb/s and up to 3.2 Gb/s, digital visual interface (DVI), USB3.0 power and data lines protection, notebook and personal computers, monitors and flat panel displays, IEEE 1394 Firewire Ports, etc.

ESD14N5V0U6U incorporates a pair of rail-to-rail diodes with low capacitance for each of four I/O channels. Additional Zener diode is employed to minimize the influence of supply voltage. The ESD protection of TVS arrays meets the immunity standard of IEC 61000-4-2, level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

DFN-10-4.1X2X0.5-0.80



PIN CONFIGURATION



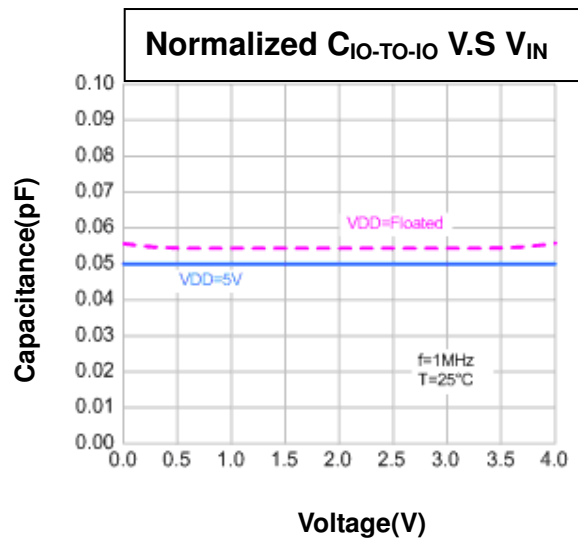
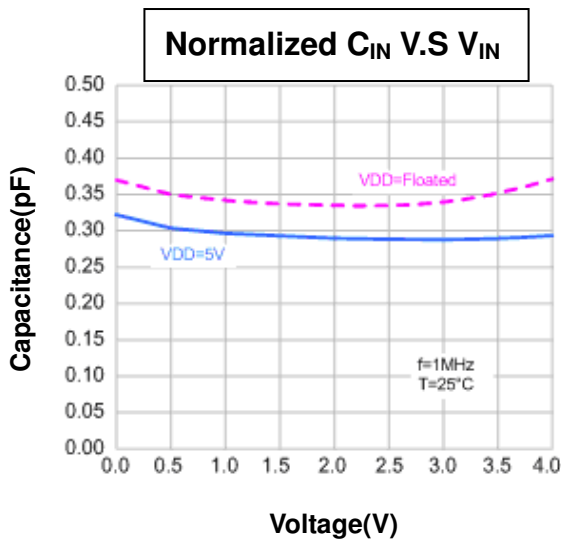
Shipping

3000/Tape&Reel

| PARAMETER | PARAMETER | RATING | UNITS |
|--|---------------|---------------|--------------------|
| Peak Pulse power ($t_p = 8/20\mu\text{s}$) | P_{pp} | 150 | W |
| Peak Pulse current ($t_p = 8/20\mu\text{s}$) | I_{pp} | 5 | A |
| Operating Supply Voltage (VDD-GND) | V_{DC} | 5 | V |
| ESD per IEC 61000-4-2 (Air) (I/O pins) | V_{ESD_IO} | 15 | kV |
| ESD per IEC 61000-4-2 (Contact) (I/O pins) | | 8 | |
| Lead Soldering Temperature | T_{SOL} | 260 (10 sec.) | $^{\circ}\text{C}$ |
| Operating Temperature | T_{OP} | -55 to +125 | $^{\circ}\text{C}$ |
| Storage Temperature | T_{STO} | -55 to +150 | $^{\circ}\text{C}$ |

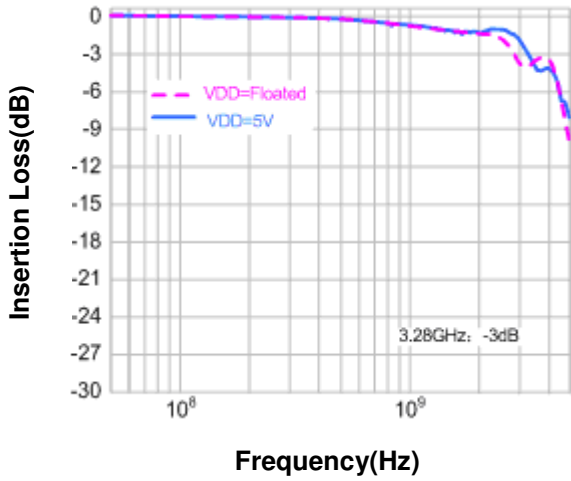


| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|------------|---|-----|-----|------|---------|
| Reverse Stand-Off Voltage | V_{RWM} | Any I/O pin to Ground | | | 5 | V |
| Reverse Leakage Current | I_{Leak} | $V_{RWM} = 5V$, Any I/O pin to Ground | | | 1 | μA |
| Reverse Breakdown Voltage | V_{BV} | $I_{BV} = 1mA$, Any I/O pin to Ground | 6 | | | V |
| ESD Clamping Voltage -I/O | V_{C1} | $I_{PP}=1A$, $t_p=8/20\mu S$, Any I/O pin to Ground | | 8.5 | 12 | V |
| Reverse ESD Clamping Voltage -I/O | V_{C2} | $I_{PP}=1A$, $t_p=8/20\mu S$, Any I/O pin to Ground | | 1.8 | | V |
| Channel to Channel Input Capacitance | C_{J1} | $V_R=0V$, $f=1MHz$ | | 0.2 | 0.25 | pF |
| Channel I/O to GND Capacitance | C_{J2} | $V_R=0V$, $f=1MHz$, Any I/O pin to Ground | | | 0.4 | pF |

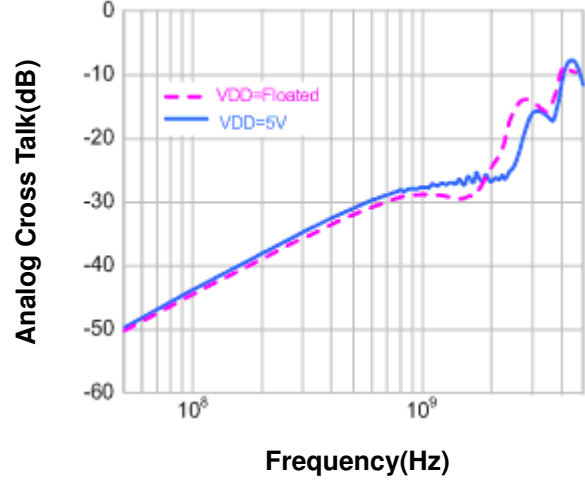




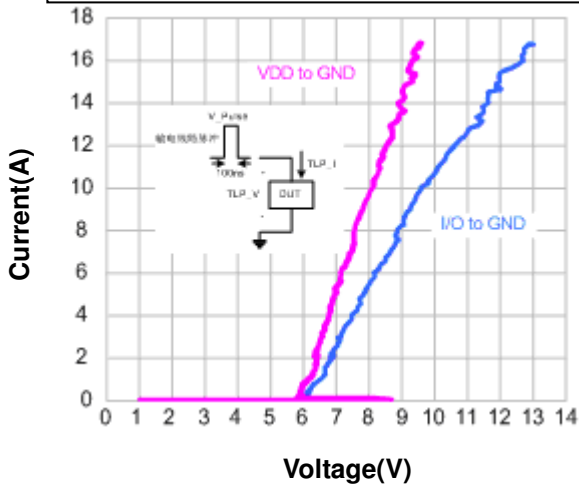
Insertion Loss S21 (I/O to Gnd)



Analog Cross

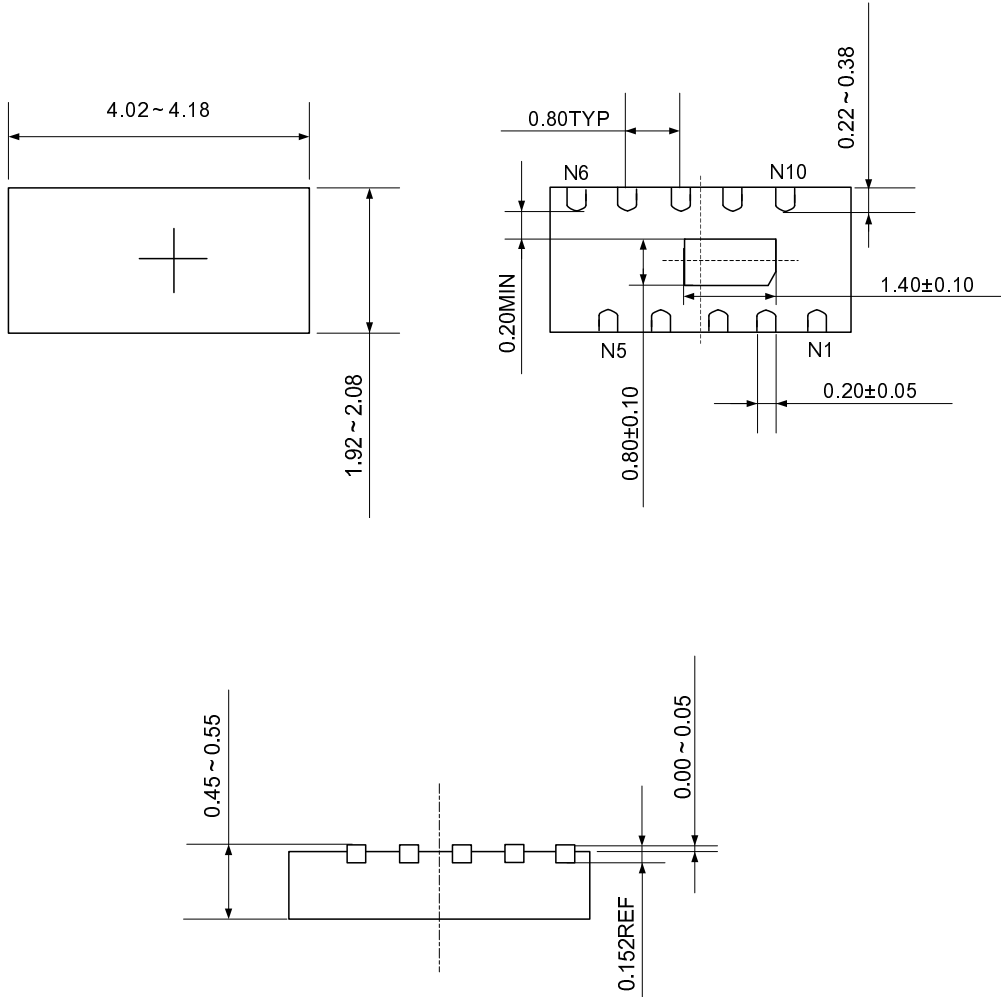


Transmission Line Pulsing (TLP)





Mechanical Details





NOTICE

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